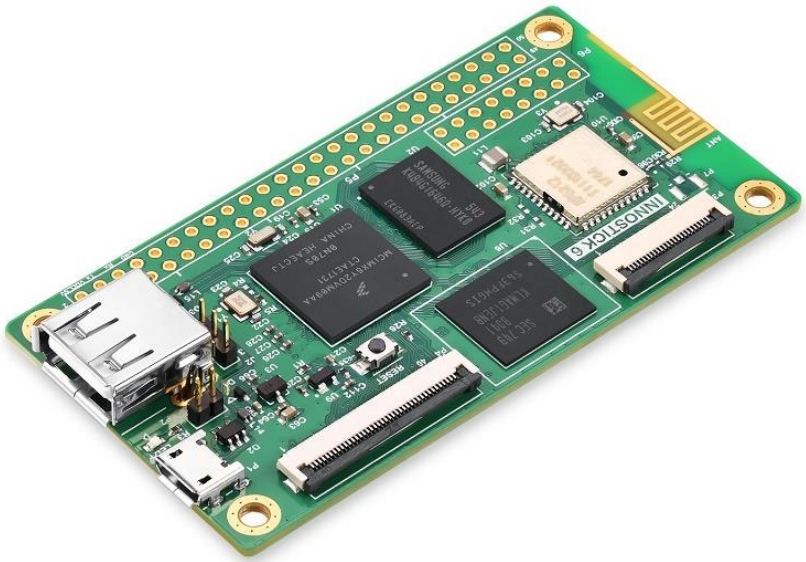
Shanghai Naxing Electronics Co., Ltd.

INNNOSTICK 6 Computer Board

Hardware Manual Rev. 1.0



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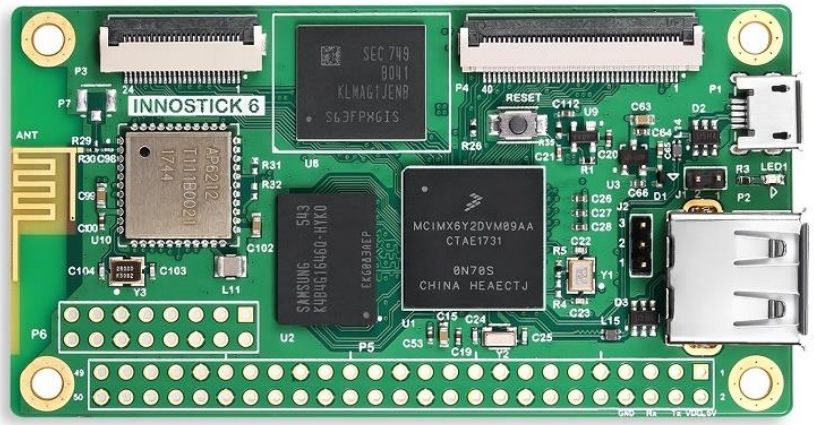
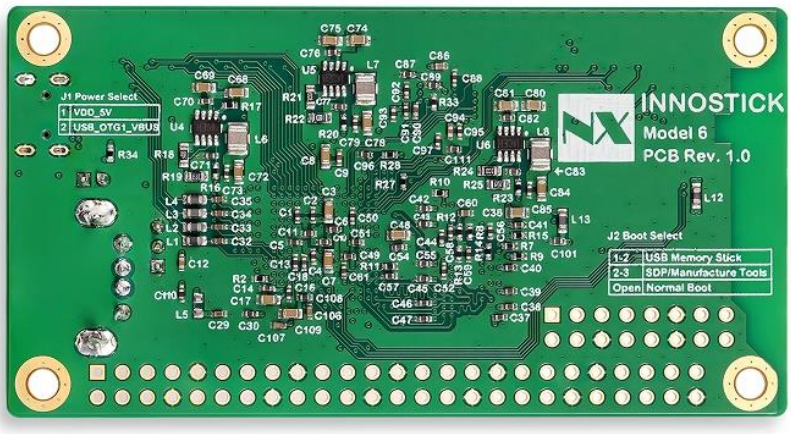
1. Overview

Based on NXP/Freescale's i.MX6ULL ARM Cortex-A7 processor with up to 900MHz CPU Clock, the INNOSTICK 6 is a portable and easy-to-use computer which integrated with on board DDR3 memory and eMMC storage in a tiny form factor(80mmx42mm).
The INNOSTICK 6 provides a variety of interfaces and connectivity options - all packaged at an optimized power, size and cost. The INNOSTICK 6 highly integrated connectivity includes Wi-Fi, Bluetooth/BLE, USB Host and OTG, Camera, LCD display with touch panel and serial interfaces.



INNOSTICK 6 Front View

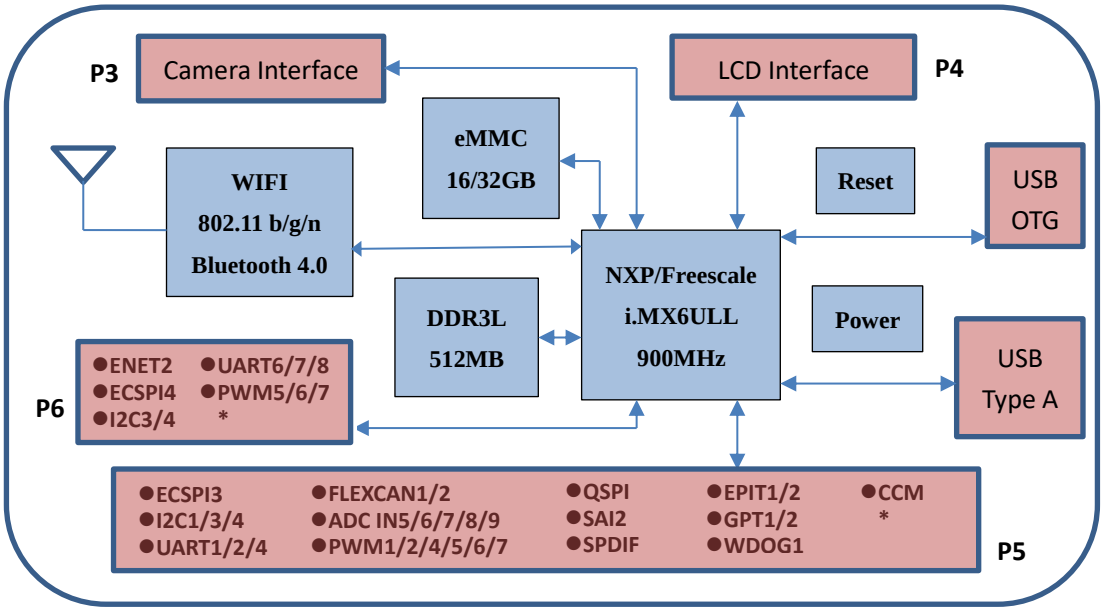


INNOSTICK 6 Back View

1.1 Hardware Features

- Processor — NXP i.MX6 ULL, 1x Cortex-A7 @ 900MHz
- Memory/Storage — 512MB DDR3L; 16GB or 32GB eMMC
- Wireless — 802.11b/g/n with Bluetooth 4.0 (AP6212 module)
- Display/Camera:
  - ✓ 24-bit RGB LCD interface with 4-wire resistive touch support
  - ✓ 8-bit CSI Parallel input
- Other I/O:
  - ✓ USB 2.0 Type A Host port
  - ✓ Micro-USB 2.0 OTG port
  - ✓ 16-pin expansion header — ENET2, ECSPI4, I2C3/4, UART6/7/8, PWM5/6/7
  - ✓ 50-pin expansion header — ECSPI3, I2C1/3/4, UART1/2/4, FLEXCAN1/2, ADC IN5/6/7/8/9, PWM1/2/4/5/6/7, QSPI, SAI2, SPDIF, EPIT1/2, GPT1/2, WDOG1, CCM
- Other features:
  - ✓ 1x User LED
  - ✓ 1x Reset Button
  - ✓ Boot and Power Jumpers
- Dimensions — 80 x 42mm
- RoHS Compliant

1.2 Block Diagram



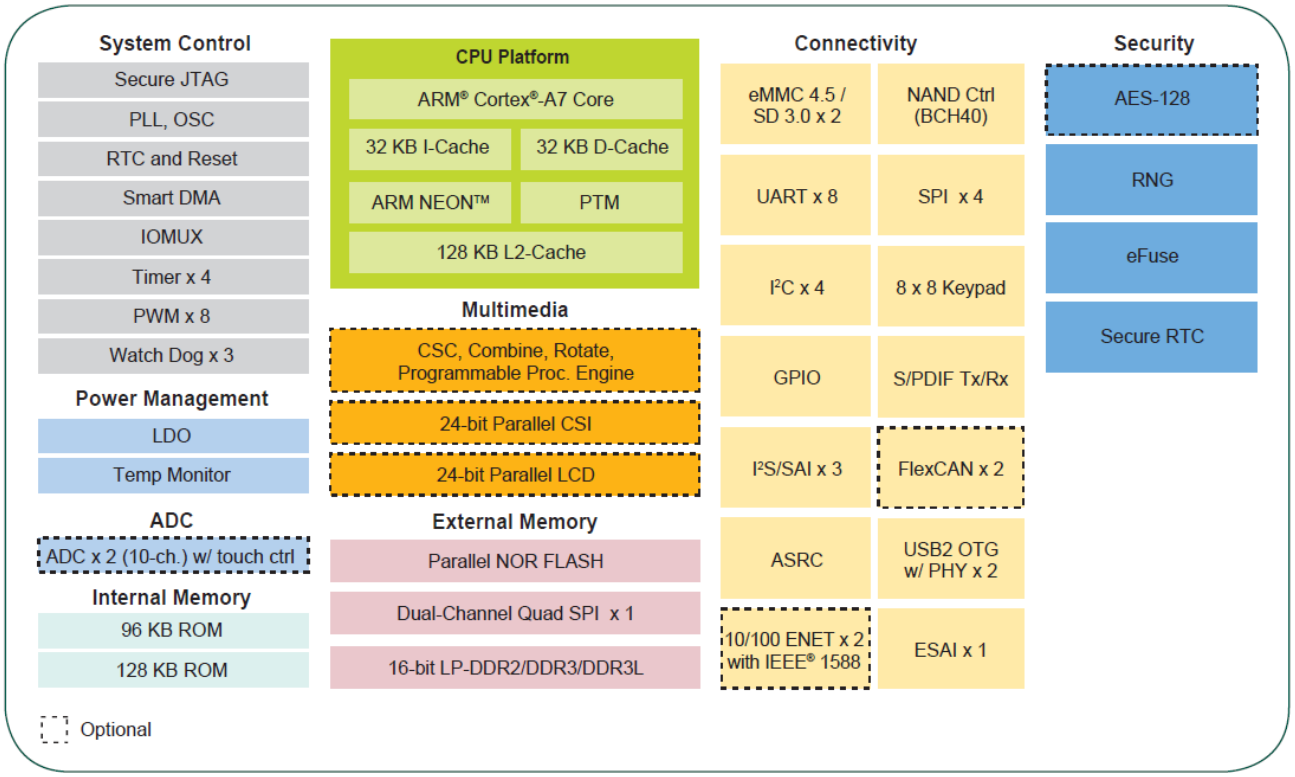
*Note：Functions may not be simultaneously available due to pin mux restriction

Functional Block Diagram

2. Hardware Functions

2.1 i.MX6ULL SOC

The i.MX 6ULL is a high performance, ultra efficient processor family with featuring NXP's advanced implementation of the single Arm Cortex®-A7 core, which operates at speeds of up to 900 MHz. i.MX 6ULL includes integrated power management module that reduces the complexity of external power supply and simplifies the power sequencing. Each processor in this family provides various memory interfaces, including LPDDR2, DDR3, DDR3L, Raw and Managed NAND flash, NOR flash, eMMC, Quad SPI, and a wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors.



i.MX6ULL Block Diagram

The features of the i.MX 6ULL processors include:

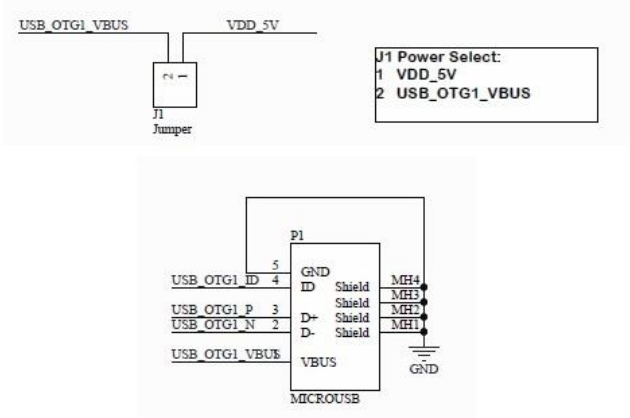
- Single-core Arm Cortex-A7—The single core A7 provides a cost-effective and power-efficient solution.
- Multilevel memory system—The multilevel memory system of processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processor supports many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, NAND Flash (MLC and SLC), OneNAND™, Quad SPI, and managed NAND, including eMMC up to rev 4.4/4.41/4.5.
- Smart speed technology—Power management implemented throughout the IC that enables multimedia features and peripherals to consume minimum power in both active and various low power modes.

- Dynamic voltage and frequency scaling—The power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of processor is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, a programmable smart DMA (SDMA) controller, an asynchronous audio sample rate converter, an Electrophoretic Display (EPD) controller, and a Pixel processing pipeline (PXP) to support 2D image processing, including color-space conversion, scaling, alpha-blending, and rotation.
- 2x Ethernet interfaces—2x 10/100 Mbps Ethernet controllers.
- Human-machine interface—Each processor supports one digital parallel display interface.
- Interface flexibility—Each processor supports connections to a variety of interfaces: two high-speed USB on-the-go with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), two 12-bit ADC modules with up to 10 total input channels and two CAN ports.
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, AES-128 encryption, SHA-1, SHA-256 HW acceleration engine, and secure software downloads.
- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

2.2 System Power

2.2.1 Main Power Supply Selection

INNOSTICK 6 main power supply VDD_5V is a single DC 5V input, which can be either supplied from Micro-USB connector (P1-1) or Expansion Header(P5-1 and P5-2). An on board Jumper J1 is used for power selection.



Main Power Supply

When Jumper J1 mounted, VDD_5V will be connected to USB_OGT1_VBUS(P1-1) which means Main Power will be supplied from Micro-USB connection.

When Jumper J1 open, VDD_5V will be disconnected from USB_OGT1_VBUS(P1-1) which means

Main Power Supply will be from Expansion Header P5-1 and P5-2.

2.2.2 On Board DC Rails

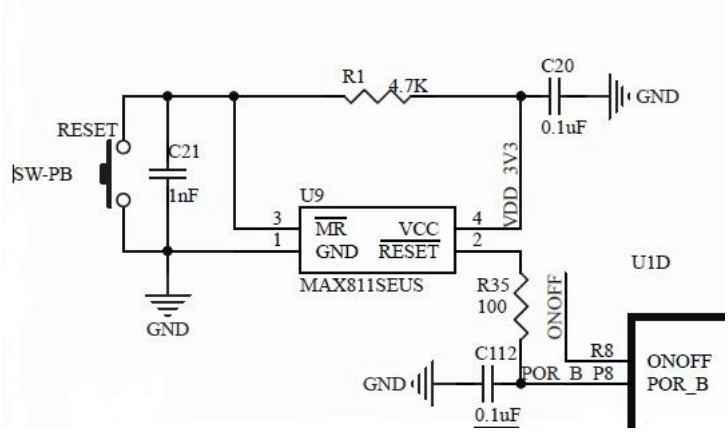
There are several DC rails exist to supply i.MX6ULL SOC and various on board peripherals.

Power On Sequence	Source From	Voltage Output	i.MX6ULL Power Rail	Description
1	VDD_5V	VDD_SNVS_3V3	VDD_SNVS_IN	SNVS_LP supply, will be constant on with Main Power Supply
2	VDD_5V	VDD_3V3	VDDHIGH_IN NVCC_XXX	DC 3.3V Output, controlled by PMIC_ON_REQ from SNVS_LP
3	VDD_5V	VDD_1V2	VDDSOC_IN	Power supply for i.MX6ULL SOC, controlled by VDD_3V3_PG
3	VDD_5V	VDD_1V35	NVCC_DRAM	Power supply for on board DDR3 memory, controlled by VDD_3V3_PG
	USB_OTG1_VBUS	USB_OTG1_VBUS	USB_OTG1_VBUS	USB_OTG1_VBUS can be chosen as Main Power Supply through Jumper J1
	VDD_5V	VDD_5V	USB_OTG2_VBUS	Directly shorted to Main Power Supply
	VDD_3V3	VDDA_3V3	VDDA_ADC_3P3	Analog to Digital Converter Supply, connected to VDD_3V3 by a 0ohm resistor

Table 2-1 On Board DC Rails

2.3 Reset

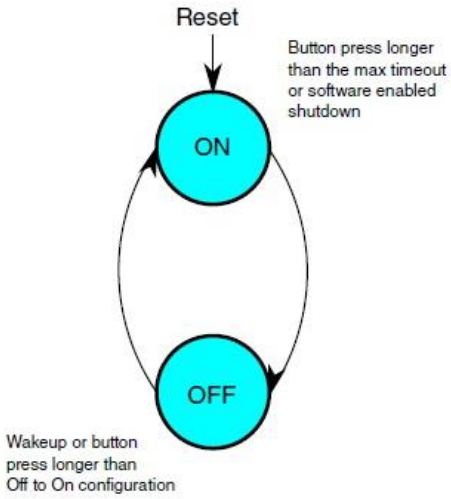
A MAX811 reset controller is used to generate global power on reset signal to i.MX6ULL SOC.



Power On Reset

2.4 ONOFF Mechanism

An ONOFF Mechanism can be achieved in SNVS_LP domain, combined with i.MX6ULL SOC ONOFF and PMIC_ON_REQ signals.



ONOFF Mechanism

2.5 Boot Configuration

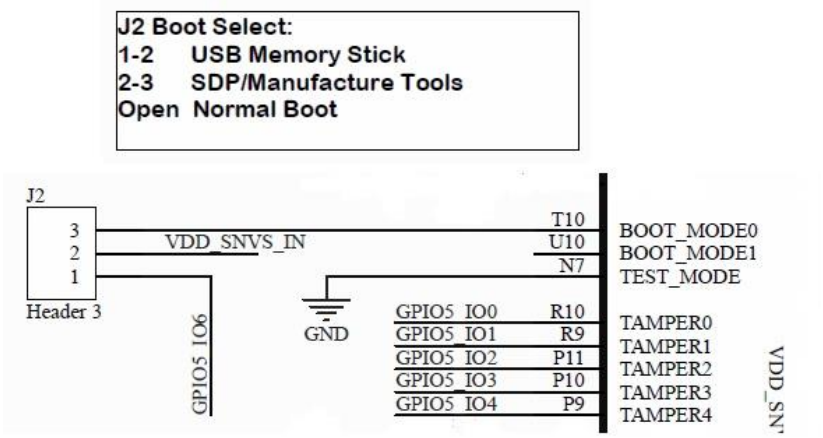
i.MX6ULL SOC has 4 boot modes which can be configured by 2 external pads—BOOT_MODE0 and BOOT_MODE1. INNOSTICK 6 only implements 2 of those 4 boot modes for board boot up.

Boot Mode[1：0]	Boot Type
00	Boot From eFuse
01	Serial Downloader
10	
11	

Table 2-2 Boot Mode

When Jumper J2-2 and J2-3 open, i.MX6ULL internal boot mode register will be set to ‘00’ since there are 2 internal pull down resistors tied to BOOT_MODE0 and BOOT_MODE1 pads. In this mode, i.MX6ULL internal Boot ROM will choose boot device through internal eFuse setting[1].
When Jumper J2-2 and J2-3 shorted, i.MX6ULL boot mode register will be set to ‘01’. In this mode, i.MX6ULL internal Boot ROM will enter Serial Download mode and try to connect with NXP/Freescale Manufacture Tools from USB Host side.

[1] Refer to i.MX 6ULL Applications Processor Reference Manual Section 8.2.3 for more details



Boot Mode

There is another GPIO pin GPIO5_IO6 routed to on board Jumper J2-1. This GPIO pin provides additional software options when user program boot up.

2.6 Memory

The i.MX6ULL Multi-Mode DDR Controller is a dedicated interface to DDR3/DDR3L/LPDDR2 SDRAM. INNOSTICK 6 support DDR3 memory in following specification.

Type	Package	Voltage	Chip Selects	Bus Width	Clock Frequency	Channel Number	Capacitance
DDR3	96 Ball FBGA	1.5V	1~2	16	400MHz	1	128MB~1GB
DDR3L	96 Ball FBGA	1.35V	1~2	16	400MHz	1	128MB~1GB

Table 2-3 DDR3 Support

All two i.MX6ULL MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are:

- Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.5/4.2/4.3/4.4/4.41/ including high-capacity (size > 2 GB) cards HC MMC.
- Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDXC cards up to 2 TB.
- Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0

Two ports support:

- 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max)
- 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max)

However, the SoC level integration and I/O muxing logic restrict the functionality to the following:

- Instances #1 and #2 are primarily intended to serve as interfaces to on-board peripherals. These ports are equipped with “Card detection” and “Write Protection” pads and do not support hardware reset.
- All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD Interface).

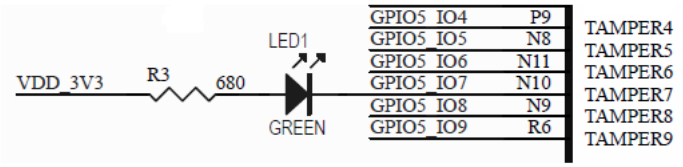
INNOSTICK 6 support eMMC in following specification.

Type	Package	Voltage	Bus Width	Clock Frequency	Capacitance
eMMC	153 Ball FBGA	3.3V	8	HS200	4GB~32GB
eMMC	169 Ball FBGA	3.3V	8	HS200	4GB~32GB

Table 2-4 eMMC Support

2.7 User LED

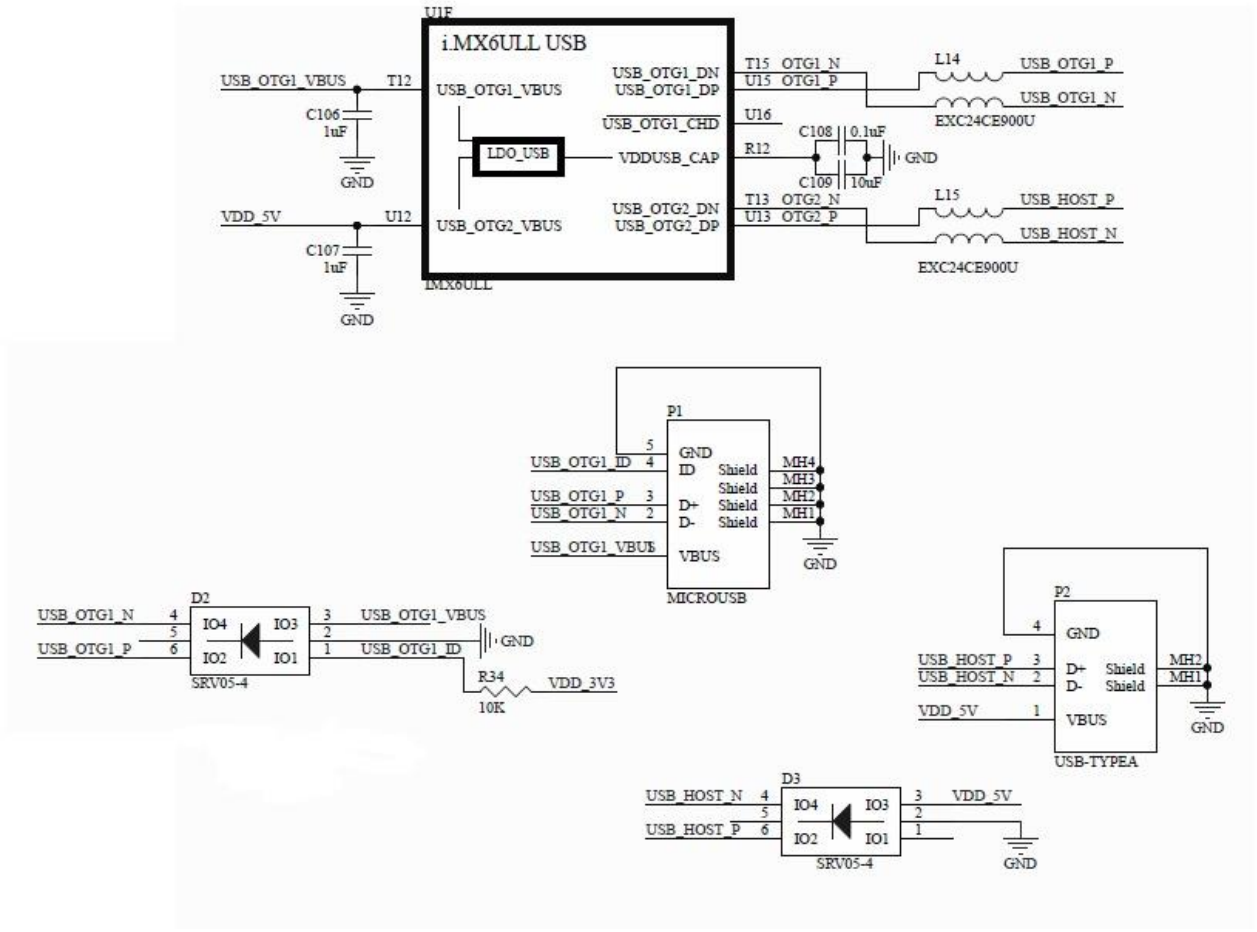
An on board LED can be used by software for status indication.



User LED

2.8 USB Interface

i.MX6ULL USB controller consists of independent USB controller cores: two On-The-Go(OTG) controller cores. Each controller core supports UTMI interface. Controller cores are single-port cores. For the OTG cores, there is only one port. The port can be used as either a downstream or an upstream port.

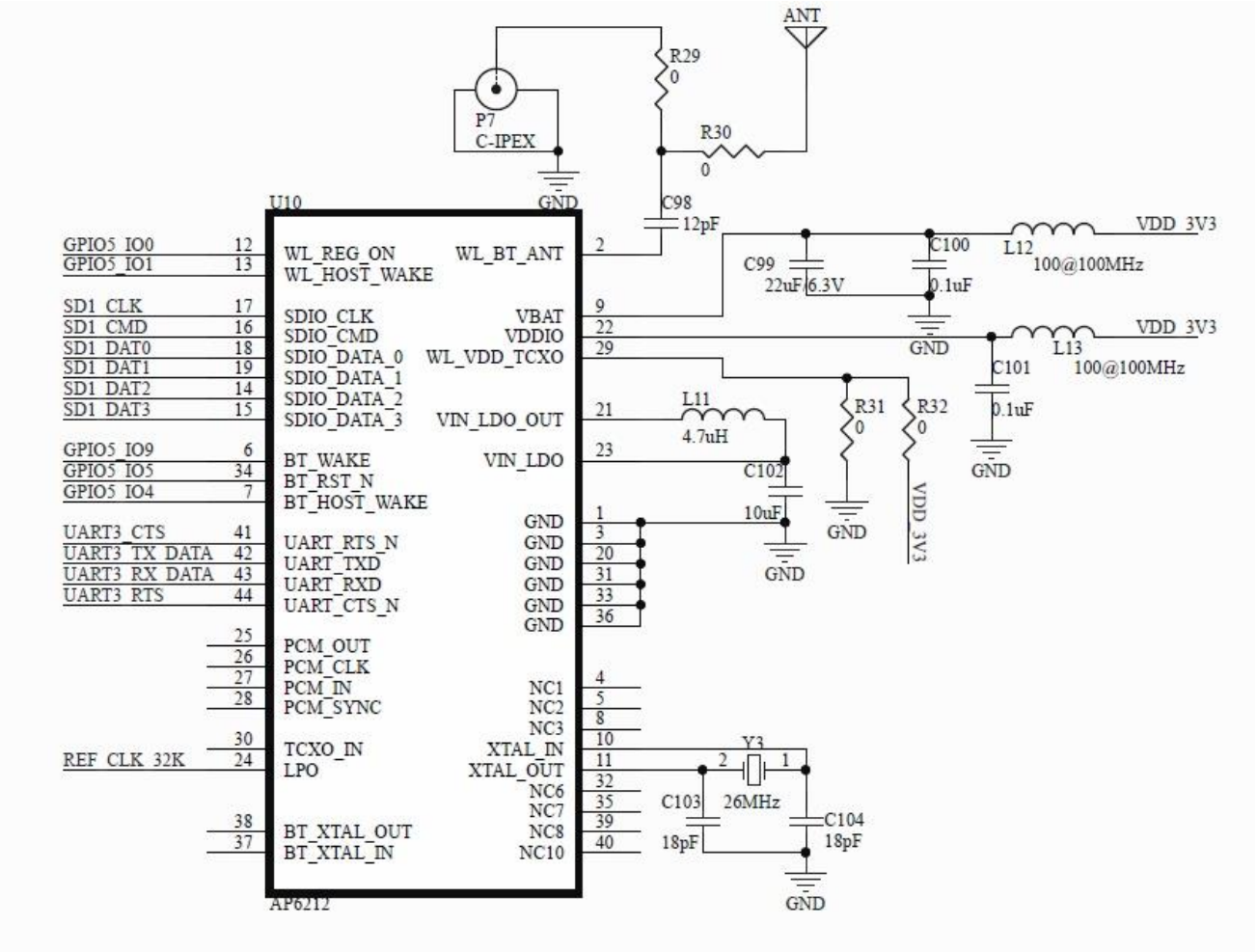


USB Interface

In INNNOSTICK 6, USB_OTG1 is implemented as a USB 2.0 OTG port(P1), USB_OTG2 is implemented as a USB 2.0 Host port(P2).

2.9 WiFi and Bluetooth

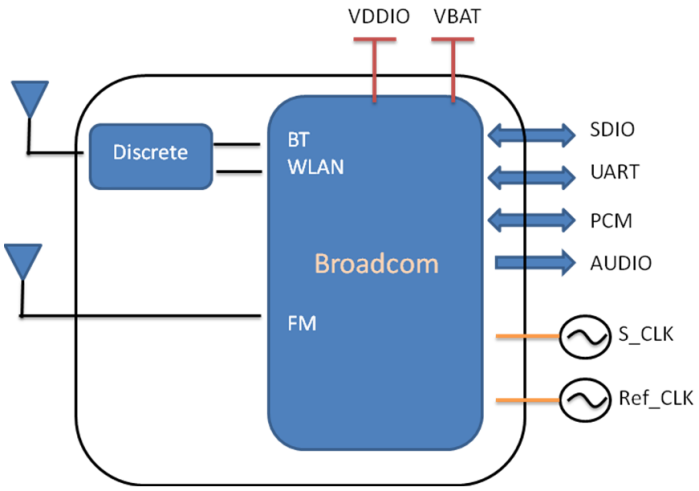
INNOSTICK6 contains an on board WiFi/BT Module, which is AP6212 from APAMK, together with an on board PCB antenna to provide WiFi and Bluetooth functions. Meanwhile a footprint of IPEX socket P7 is left for option of external antenna connection. The WiFi part of AP6212 is connected to i.mx6ULL SDIO1 interface and Bluetooth part is connected to i.MX6ULL UART3.



WiFi and Bluetooth

APMAK AP6212 Introduction

AP6212 is a low-cost and low-power consumption module which has all of the WiFi, Bluetooth and FM functionalities. The highly integrated module makes the possibilities of web browsing, VoIP, Bluetooth headsets, FM radio functional applications and other applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11b/g/n Access Points in the wireless LAN.



AP6212 Block Diagram

APMAK AP6212 Features

- 802.11b/g/n single-band radio
- Bluetooth V4.0(HS) with integrated Class 1.5 PA and Low Energy (BLE) support
- Concurrent Bluetooth, FM (RX) RDS/RBDS, and WLAN operation
- Simultaneous BT/WLAN receive with single antenna
- WLAN host interface options:
  - ✓ SDIO v2.0 — up to 50 MHz clock rate
- BT host digital interface:
  - ✓ UART (up to 4 Mbps)
- FM multiple audio routing options: I2S, PCM, eSCO, A2DP
- IEEE Co-existence technologies are integrated die solution
- ECI — enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

2.10 LCD Interface

The i.MX6ULL eLCDIF is a general purpose display controller used to drive a wide range of display devices varying in size and capability.
The eLCDIF block supports the following:

- Displays with an asynchronous parallel MPU interface for command and data transfer to an integrated frame buffer.
- Displays that support moving pictures and require the RGB interface mode (DOTCLK interface).
- VSYNC mode for high-speed data transfers.
- Digital video encoders that accept ITU-R BT.656 format 4:2:2 YCbCr digital component video and convert it to analog TV signals.

INNOSTICK 6 provides an 24 Bits LCD interface on a 40pin 0.5mm FPC Connector(P4)

Pin#	Signal (Ball Name)	Power Domain	Description
1	TSYP	VDDA_3V3	Connect to Analog to Digital Converter 1 channel 2
2	TSYM	VDDA_3V3	Connect to Analog to Digital Converter 1 channel 1
3	TSXP	VDDA_3V3	Connect to Analog to Digital Converter 1 channel 3
4	TSXM	VDDA_3V3	Connect to Analog to Digital Converter 1 channel 4
5	GND	-	Ground
6	LCD_HSYNC	VDD_3V3	LCD horizontal sync
7	LCD_VSYNC	VDD_3V3	LCD vertical sync
8	LCD_ENABLE	VDD_3V3	LCD enable
9	GND		Ground
10	LCD_RESET	VDD_3V3	LCD reset
11	PWM8	VDD_3V3	PWM output 8
12	LCD_CLK	VDD_3V3	LCD Pixel Clock
13	LCD_DAT23	VDD_3V3	LCD Pixel Data bit 23
14	LCD_DAT22	VDD_3V3	LCD Pixel Data bit 22
15	LCD_DAT21	VDD_3V3	LCD Pixel Data bit 21
16	LCD_DAT20	VDD_3V3	LCD Pixel Data bit 20
17	LCD_DAT19	VDD_3V3	LCD Pixel Data bit 19
18	LCD_DAT18	VDD_3V3	LCD Pixel Data bit 18
19	LCD_DAT17	VDD_3V3	LCD Pixel Data bit 17
20	LCD_DAT16	VDD_3V3	LCD Pixel Data bit 16
21	GND	-	Ground
22	LCD_DAT15	VDD_3V3	LCD Pixel Data bit 15
23	LCD_DAT14	VDD_3V3	LCD Pixel Data bit 14
24	LCD_DAT13	VDD_3V3	LCD Pixel Data bit 13
25	LCD_DAT12	VDD_3V3	LCD Pixel Data bit 12
26	LCD_DAT11	VDD_3V3	LCD Pixel Data bit 11
27	LCD_DAT10	VDD_3V3	LCD Pixel Data bit 10
28	LCD_DAT9	VDD_3V3	LCD Pixel Data bit 9
29	LCD_DAT8	VDD_3V3	LCD Pixel Data bit 8
30	GND	-	Ground
31	LCD_DAT7	VDD_3V3	LCD Pixel Data bit 7
32	LCD_DAT6	VDD_3V3	LCD Pixel Data bit 6
33	LCD_DAT5	VDD_3V3	LCD Pixel Data bit 5
34	LCD_DAT4	VDD_3V3	LCD Pixel Data bit 4
35	LCD_DAT3	VDD_3V3	LCD Pixel Data bit 3
36	LCD_DAT2	VDD_3V3	LCD Pixel Data bit 2
37	LCD_DAT1	VDD_3V3	LCD Pixel Data bit 1
38	LCD_DAT0	VDD_3V3	LCD Pixel Data bit 0
39	VDD_5V	-	DC rail from the Main power supply
40	VDD_5V	-	DC rail from the Main power supply

Table 2-5 LCD Interface P4

2.11 Camera Interface

The i.MX6ULL CSI IP provides parallel CSI standard camera interface port. The CSI parallel data ports are up to 24 bits. It is designed to support 24-bit RGB888/YUV444, CCIR656 video interface, 8-bit YCbCr, YUV or RGB, and 8-bit/10-bit/16-bit Bayer data input.
INNOSTICK 6 provides an 8 Bits Camera interface on a 24pin 0.5mm FPC Connector(P3)

Pin #	Signal (Ball Name)	Power Domain	Description
1	VDD_3V3	VDD_3V3	DC 3.3V Output
2	VDD_3V3	VDD_3V3	DC 3.3V Output
3	I2C2_SCL	VDD_3V3	I2C2 clock
4	I2C2_SDA	VDD_3V3	I2C2 data
5	GPIO5_IO8	VDD_3V3	
6	GPIO5_IO3	VDD_3V3	
7	GND		Ground
8	CSI_MCLK	VDD_3V3	CSI MCLK
9	GND		Ground
10	GND		Ground
11	CSI_VSYNC	VDD_3V3	CSI vertical sync
12	CSI_HSYNC	VDD_3V3	CSI horizontal sync
13	GND		Ground
14	CSI_PIXCLK	VDD_3V3	CSI pixel clock
15	GND		Ground
16	CSI_DATA07	VDD_3V3	CSI data 7
17	CSI_DATA06	VDD_3V3	CSI data 6
18	CSI_DATA05	VDD_3V3	CSI data 5
19	CSI_DATA04	VDD_3V3	CSI data 4
20	CSI_DATA03	VDD_3V3	CSI data 3
21	CSI_DATA02	VDD_3V3	CSI data 2
22	CSI_DATA01	VDD_3V3	CSI data 1
23	CSI_DATA00	VDD_3V3	CSI data 0
24	GND		Ground

Table 2-6 Camera Interface P3

2.12 Expansion Headers

i.MX6ULL SOC is packaged in a 289 pins 0.8mm BGA chip. Besides the pins occupied by on board peripherals like eMMC, WiFi/BT, and other pins belong to LCD and Camera interfaces, all the rest GPIO pins are routed to two 2.54mm pitch through-hole pin headers, which named as Expansion Header P5 and Expansion Header P6.

2.12.1 Expansion Header P5

INNOSTICK 6 provides a 2x25 pin 2.54mm pitch Expansion Header(P5).

Power Domain	i.MX6ULL Alt5 Mode[2]	Signal (Ball Name)	Pin#		Signal (Ball Name)	i.MX6ULL Alt5 Mode[2]	Power Domain
Main Power Supply		VDD_5V	1	2	VDD_5V		Main Power Supply
DC 3.3V Output		VDD_3V3	3	4	UART1_TX_DATA	GPIO1_IO16	VDD_3V3
VDD_3V3	GPIO1_IO19	UART1_RTS_B	5	6	UART1_RX_DATA	GPIO1_IO17	VDD_3V3
VDD_3V3	GPIO1_IO18	UART1_CTS_B	7	8	GND		
		GND	9	10	VDDA_3V3		Analog Converter Supply
VDD_3V3	GPIO1_IO05	GPIO1_IO05	11	12	GPIO1_IO06	GPIO1_IO06	VDD_3V3
VDD_3V3	GPIO1_IO07	GPIO1_IO07	13	14	GPIO1_IO08	GPIO1_IO08	VDD_3V3
VDD_3V3	GPIO1_IO09	GPIO1_IO09	15	16	GND		
		GND	17	18	JTAG_TDI	GPIO1_IO13	VDD_3V3
VDD_3V3	GPIO1_IO10	JTAG_MOD	19	20	JTAG_TDO	GPIO1_IO12	VDD_3V3
VDD_3V3	GPIO1_IO15	JTAG_TRSTB	21	22	JTAG_TCK	GPIO1_IO14	VDD_3V3
VDD_3V3	GPIO1_IO11	JTAG_TMS	23	24	GND		
		GND	25	26	SNVS_TAMPER2	GPIO5_IO02	VDD_SNVS_IN
SNVS_LP Supply		VDD_SNVS_IN	27	28	PMIC_STBY_REQ		VDD_SNVS_IN
VDD_SNVS_IN		PMIC_ON_REQ	29	30	ONOFF		VDD_SNVS_IN
VDD_SNVS_IN		POR_B	31	32	GND		
		GND	33	34	NAND_READY_B	GPIO4_IO11	VDD_3V3
VDD_3V3	GPIO4_IO12	NAND_WP_B	35	36	NAND_CE0_B	GPIO4_IO13	VDD_3V3
VDD_3V3	GPIO4_IO14	NAND_CE1_B	37	38	NAND_CLE	GPIO4_IO15	VDD_3V3
VDD_3V3	GPIO4_IO16	NAND_DQS	39	40	GND		
		GND	41	42	ENET1_RX_DATA1	GPIO2_IO01	VDD_3V3
VDD_3V3	GPIO2_IO00	ENET1_RX_DATA0	43	44	UART4_RX_DATA	GPIO1_IO29	VDD_3V3
VDD_3V3	GPIO1_IO28	UART4_TX_DATA	45	46	UART2_RTS_B	GPIO1_IO23	VDD_3V3

[2] Refer to Section 2.12.3 for more Alt Modes

VDD_3V3	GPIO1_IO21	UART2_RX_DATA	47	48	UART2_CTS_B	GPIO1_IO22	VDD_3V3
VDD_3V3	GPIO1_IO20	UART2_TX_DATA	49	50	GND		

Table 2-7 Expansion Header P5

2.12.2 Expansion Header P6

INNOSTICK 6 provides a 2x8 pin 2.54mm pitch Expansion Header(P6).

Power Domain	i.MX6ULL Alt5 Mode[3]	Signal (Ball Name)	Pin#		Signal (Ball Name)	i.MX6ULL Alt5 Mode[3]	Power Domain
DC 3.3V Output		VDD_3V3	1	2	ENET1_TX_CLK	GPIO2_IO06	VDD_3V3
VDD_3V3	GPIO2_IO03	ENET1_TX_DATA0	3	4	ENET1_TX_DATA1	GPIO2_IO04	VDD_3V3
VDD_3V3	GPIO2_IO05	ENET1_TX_EN	5	6	GND		
VDD_3V3	GPIO2_IO11	ENET2_TX_DATA0	7	8	ENET2_TX_DATA1	GPIO2_IO12	VDD_3V3
VDD_3V3	GPIO2_IO13	ENET2_TX_EN	9	10	ENET2_TX_CLK	GPIO2_IO14	VDD_3V3
		GND	11	12	GND		
VDD_3V3	GPIO2_IO10	ENET2_RX_EN	13	14	ENET2_RX_DATA1	GPIO2_IO09	VDD_3V3
VDD_3V3	GPIO2_IO15	ENET2_RX_ER	15	16	ENET2_RX_DATA0	GPIO2_IO08	VDD_3V3

Table 2-8 Expansion Header P6

2.12.3 Expansion Pin MUX

The i.MX6ULL SOC contains a limited number of pins, most of which have multiple signal options. These signal-to-pin and pin-to-signal options are selected by the input-output multiplexer called IOMUX. The IOMUX is also used to configure other pin characteristics, such as voltage level, drive strength, and hysteresis.
The muxing options table lists the external signals grouped by the module instance, the muxing options for each signal, and the registers used to route the signal to the chosen pad.

IP Instance	Port Name	Pin#	Signal(Ball Name)	Mode
CCM	CLKO1	P5-23	JTAG_TMS	ALT3
	CLKO2	P5-20	JTAG_TDO	ALT3
	PMIC_READY	P5-14	GPIO1_IO08	ALT6
		P5-19	JTAG_MOD	ALT4
	PMIC_STBY_REQ	P5-28	PMIC_STBY_REQ	
ECSPI3	MISO	P5-38	NAND_CLE	ALT3
		P5-46	UART2_RTS	ALT8
	MOSI	P5-37	NAND_CE1_B	ALT3
		P5-48	UART2_CTS	ALT8
	RDY	P5-35	NANDF_WP_B	ALT8

[3] Refer to Section 2.12.3 for more Alt Modes

IP Instance	Port Name	Pin#	Signal(Ball Name)	Mode
	SCLK	P5-36	NAND_CE0_B	ALT3
		P5-47	UART2_RX_DATA	ALT8
	SS0	P5-34	NAND_READY_B	ALT3
		P5-49	UART2_TX_DATA	ALT8
ECSPI4	MISO	P6-10	ENET2_TX_CLK	ALT3
	MOSI	P6-9	ENET2_TX_EN	ALT3
	SCK	P6-8	ENET2_TX_DATA1	ALT3
	SS0	P6-15	ENET2_RX_ER	ALT3
ENET2	MDC	P6-5	ENET1_TX_EN	ALT4
		P5-13	GPIO1_IO07	ALT1
	MDIO	P6-4	ENET1_TX_DATA1	ALT4
		P5-12	GPIO1_IO06	ALT1
	RDATA0	P6-16	ENET2_RX_DATA0	ALT0
	RDATA1	P6-14	ENET2_RX_DATA1	ALT0
	RX_EN	P6-13	ENET2_RX_EN	ALT0
	RX_ER	P6-15	ENET2_RX_ER	ALT0
	TDATA0	P6-7	ENET2_TX_DATA0	ALT0
	TDATA1	P6-8	ENET2_TX_DATA1	ALT0
	TX_CLK	P6-10	ENET2_TX_CLK	ALT0
	TX_EN	P6-9	ENET2_TX_EN	ALT0
EPIT1	OUT	P5-23	JTAG_TMS	ALT8
EPIT2	OUT	P5-20	JTAG_TDO	ALT8
FLEXCAN1	RX	P5-42	ENET1_RX_DATA1	ALT4
	TX	P5-43	ENET1_RX_DATA0	ALT4
FLEXCAN2	RX	P6-3	ENET1_TX_DATA0	ALT4
		P5-46	UART2_RTS	ALT2
	TX	P5-48	UART2_CTS	ALT2
GPT1	CAPTURE1	P5-49	UART2_TX_DATA	ALT4
	CAPTURE2	P5-47	UART2_RX_DATA	ALT4
	CLK	P6-2	ENET1_TX_CLK	ALT8
		P5-6	UART1_RX_DATA	ALT4
	COMPARE1	P5-4	UART1_TX_DATA	ALT4
	COMPARE2	P5-48	UART2_CTS_B	ALT4
	COMPARE3	P5-46	UART2_RTS_B	ALT4
GPT2	CAPTURE1	P5-23	JTAG_TMS	ALT1
	CAPTURE2	P5-20	JTAG_TDO	ALT1
	CLK	P5-19	JTAG_MOD	ALT1
	COMPARE1	P5-18	JTAG_TDI	ALT1
	COMPARE2	P5-22	JTAG_TCK	ALT1
	COMPARE3	P5-21	JTAG_TRST_B	ALT1
I2C1	SCL	P5-45	UART4_TX_DATA	ALT2
	SDA	P5-44	UART4_RX_DATA	ALT2

IP Instance	Port Name	Pin#	Signal(Ball Name)	Mode
I2C3	SCL	P6-16	ENET2_RX_DATA0	ALT3
		P5-4	UART1_TX_DATA	ALT2
	SDA	P6-14	ENET2_RX_DATA1	ALT3
		P5-6	UART1_RX_DATA	ALT2
I2C4	SCL	P6-13	ENET2_RX_EN	ALT3
		P5-49	UART2_TX_DATA	ALT2
	SDA	P6-7	ENET2_TX_DATA0	ALT3
		P5-47	UART2_RX_DATA	ALT2
MQS	LEFT	P5-18	JTAG_TDI	ALT6
	RIGHT	P5-20	JTAG_TDO	ALT6
PWM1	OUT	P5-43	ENET1_RX_DATA0	ALT2
		P5-14	GPIO1_IO08	ALT0
PWM2	OUT	P5-42	ENET1_RX_DATA1	ALT2
		P5-15	GPIO1_IO09	ALT0
PWM4	OUT	P5-11	GPIO1_IO05	ALT1
		P5-35	NAND_WP_B	ALT3
PWM5	OUT	P6-4	ENET1_TX_DATA1	ALT2
		P5-39	NAND_DQS	ALT3
PWM6	OUT	P6-5	ENET1_TX_EN	ALT2
		P5-18	JTAG_TDI	ALT4
PWM7	OUT	P6-2	ENET1_TX_CLK	ALT2
		P5-22	JTAG_TCK	ALT4
QSPI	A_DATA0	P5-34	NAND_READY_B	ALT2
	A_DATA1	P5-36	NAND_CE0_B	ALT2
	A_DATA2	P5-37	NAND_CE1_B	ALT2
	A_DATA3	P5-38	NAND_CLE	ALT2
	A_SCLK	P5-35	NAND_WP_B	ALT2
	A_SS0_B	P5-39	NAND_DQS	ALT2
SAI2	MCLK	P5-23	JTAG_TMS	ALT2
	RX_DATA	P5-22	JTAG_TCK	ALT2
	TX_BCLK	P5-18	JTAG_TDI	ALT2
	TX_DATA	P5-21	JTAG_TRSTB	ALT2
	TX_SYNC	P5-20	JTAG_TDO	ALT2
SPDIF	EXT_CLK	P5-39	NAND_DQS	ALT8
	IN	P5-15	GPIO1_IO09	ALT2
		P5-6	UART1_RX_DATA	ALT8
	OUT	P5-14	GPIO1_IO08	ALT2
		P5-19	JTAG_MOD	ALT2
		P5-4	UART1_TX_DATA	ALT8
UART1	CTS_B	P5-12	GPIO1_IO06	ALT8
		P5-7	UART1_CTS_B	ALT0
	RTS_B	P5-13	GPIO1_IO07	ALT8

IP Instance	Port Name	Pin#	Signal(Ball Name)	Mode
		P5-5	UART1_RTS_B	ALT0
	RX_DATA	P5-6	UART1_RX_DATA	ALT0
	TX_DATA	P5-4	UART1_TX_DATA	ALT0
UART2	CTS_B	P5-48	UART2_CTS_B	ALT0
	RTS_B	P5-46	UART2_RTS_B	ALT0
	RX_DATA	P5-47	UART2_RX_DATA	ALT0
	TX_DATA	P5-49	UART2_TX_DATA	ALT0
UART4	CTS_B	P5-42	ENET1_RX_DATA1	ALT1
	RTS_B	P5-43	ENET1_RX_DATA0	ALT1
	RX_DATA	P5-44	UART4_RX_DATA	ALT0
	TX_DATA	P5-45	UART4_TX_DATA	ALT0
UART6	CTS_B	P6-4	ENET1_TX_DATA1	ALT1
	RTS_B	P6-5	ENET1_TX_EN	ALT1
	RX_DATA	P6-14	ENET2_RX_DATA1	ALT1
	TX_DATA	P6-16	ENET2_RX_DATA0	ALT1
UART7	RX_DATA	P6-7	ENET2_TX_DATA0	ALT1
	TX_DATA	P6-13	ENET2_RX_EN	ALT1
UART8	CTS_B	P6-10	ENET2_TX_CLK	ALT1
	RTS_B	P6-15	ENET2_RX_ER	ALT1
	RX_DATA	P6-9	ENET2_TX_EN	ALT1
	TX_DATA	P6-8	ENET2_TX_DATA1	ALT1
WDOG1	WDOG_ANY	P6-15	ENET2_RX_ER	ALT8
		P5-15	GPIO1_IO09	ALT1
	WDOG_B	P5-14	GPIO1_IO08	ALT1
	WDOG_RST_B_DEB	P6-4	ENET1_TX_DATA1	ALT8

Table 2-9 Expansion Pin MUX

3. Electrical Specifications

3.1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VDD_5V	Main Power Supply	-0.5	5.5	V
USB_OTG1_VBUS	USB VBUS	-	5.5	V
Vin/Vout	Input/Output Voltage Range	-0.5	OVDD+0.3[4]	V

Table 3-1 Absolute Maximum Ratings

3.2 Operating Conditions

Symbol	Description	Min	Max	Unit
VDD_5V	Main Power Supply	4.4	5.5	V
USB_OTG1_VBUS	USB VBUS	4.4	5.5	V

Table 3-2 Operating Conditions

3.3 Power Consumption

Mode	Supply	Current	Power	Note
Off	VDD_5V	120uA	0.6mW	Only SNVS_LP supplied
Standby	VDD_5V	TBD	TBD	Memory retention mode
Linux idle	VDD_5V	70mA	0.35W	
Max CPU load	VDD_5V	TBD	TBD	
Max CPU load + Max WiFi throughput	VDD_5V	TBD	TBD	

Table 3-3 Power Consumption

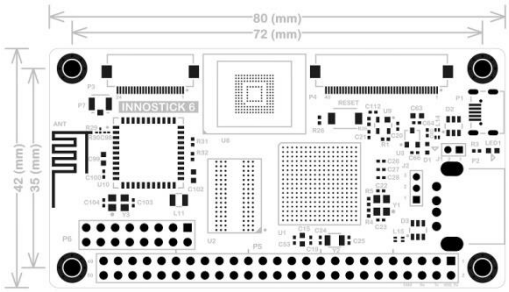
4. Environmental Specifications

Parameter	Min	Max	Unit
Commercial Operating Temperature Range	**0**	**70**	°C
Storage Temperature Range	-40	85	°C
Humidity	10	95 Non-Condensing	%

Table 4-1 Environmental Specifications

[4] OVDD is the I/O supply voltage

5. Mechanical Dimensions



Mechanical Dimensions(Top View)

6. Ordering Information

Part No.	Part Name	Operation Temp.	eMMC Size	DDR3 Size
NBD06001	INNOSTICK 6 16GB PCBA	Commercial	16GB	512MB
NBD06011	INNOSTICK 6 32GB PCBA	Commercial	32GB	512MB

Table 6-1 Ordering Information

7. Warranty Terms

Naxing Electronics guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Naxing Electronics' sole liability shall be for Naxing Electronics, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

Disclaimer of Warranty

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Technical support, email to **service@nxelec.com** or technical forum **www.esky-sh.com/bbs**(recommended)
Business and marketing, contact **market@nxelec.com**

Website **www.nxelec.com**

9. Revision History

Rev.	Date	Description	Author
0.1	25-Feb-2018	Initial release	wdzhou
1.0	14-July-2018	Release to production	wdzhou